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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,149	02/14/2002	Milivoje Aleksic	00100.02.0060(990060D-1)	7928

29153 7590 11/16/2005

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EXAMINER	
KING, JUSTIN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,149	ALEKSIC ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 18-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Iachetta, Jr. (U.S. Patent No. 5,727,171), Kelley et al. (U.S. Patent No. 6,295,568), and Heil et al. (U.S. Patent No. 5,392,407).

Referring to claim 18: Iachetta discloses a data processing system including a system controller (figure 4, structure 640) and a high–speed arbiter (figure 4, structure 710), an I/O controller (figure 4, structure 810), and a second arbiter (figure 4, structure 910). Iachetta discloses a memory system (figure 4, structure 660) connected to the system controller. Although Iachetta does not explicitly disclose the logic for controlling the memory's I/O operations, Iachetta's memory cannot function properly without one. Such memory I/O control

logic is the claimed memory control channel. Iachetta discloses that the system controller connects to a high-speed PCI bus (figure 4, structure 680), and the I/O controller connects to a low-speed PCI bus (figure 4, structure 860). Iachetta does not disclose that each arbiter is physically integrated into the system controller or the I/O controller. Iachetta also does not disclose two separate memory channels.

Kelly discloses a bridge supporting multiple frequency speeds (figure 3). Kelly's bridge has an integrated arbiter (figure 3, structure 102) to arbitrate bus access among different frequency segments. Kelly teaches one to integrate the arbiter into the bridge to arbitrate the bus according to the priority.

Heil discloses a multiple-port structure. Heil discloses two separate memory channel controllers (figure 8, structures 134, 136, 142, and 144). Heil teaches that the general access latency caused by the severe bandwidth constraint can be improved with the dual memory channels (column 1, lines 52-56).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Kelly and Heil's teachings onto Iachetta because Kelly teaches one to integrate an arbiter into the bridge to arbitrate the bus according to the each frequency segment's relative workload, and Heil teaches one to improve the general access latency by the dual memory channels.

Referring to claims 19-20: Iachetta's high-speed bus at 66 MHz is at least 10 percent faster than the low-speed bus at 33 MHz.

Referring to claim 24: Claim 18's argument applies; furthermore, Iachetta does not explicitly disclose a data storage device coupled to a bridge to transmit data at a data rate higher

than the data rate of the low-speed bus arbiter. Kelly discloses a bridge connecting with different buses with different bus speeds; thus, a data storage device, such as a CD ROM, is equivalent to the claimed data storage device when it is connected to a higher-speed bus that is coupled to the bridge.

4. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Iachetta and Kelley.

Referring to claim 22: Iachetta discloses a data processing system including a system controller and a first arbiter (figure 4, structures 640 and 710), and an I/O controller and a second arbiter (figure 4, structures of 810 and 910). Iachetta discloses that the system controller connects to a high-speed PCI bus (figure 4, structure 680), and the I/O controller connects to a low-speed PCI bus (figure 4, structure 860). The high-speed PCI bus is the claimed first bus of a predefined protocol type at a first data rate. The low-speed PCI bus is the claimed second bus. The I/O controller's connecting means to the high-speed PCI bus is the claimed control circuitry. Iachetta does not disclose that each arbiter is physically integrated into the system controller or the I/O controller.

Kelly discloses a bridge supporting multiple frequency speeds (figure 3). Kelly's bridge has an integrated arbiter (figure 3, structure 102) to arbitrate bus access among different frequency segments. Kelly teaches one to integrate the arbiter into the bridge to arbitrate the bus according to the priority.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Kelly's teachings onto Iachetta because Kelly

teaches one to integrate an arbiter into the bridge to arbitrate the bus according to the each frequency segment's relative workload.

Referring to claim 23: Iachetta discloses an I/O device (figure 4, structure 940) couple to the control circuitry of the second controller without being coupled to the arbiter of the first controller.

Response to Arguments

5. In response to Applicant's argument that the data storage device 660 of Iachetta is coupled to the host bridge 640 which is alleged to be Applicant's claimed system controller (Remark, page 4, 4th paragraph, lines 1-2): The claimed limitations in claim 18 explicitly claims a system controller having a first memory channel controller, and the Application's figure 1 depicts the storage device coupled to the system controller. Hence, Iachetta's disclosed structure does read on the claimed limitations.

6. In response to Applicant's argument that the prior arts on record fails to disclose the high speed arbiter coupled to the I/O controller (Remark, page 4, last paragraph, page 5, 1st paragraph): Iachetta discloses that the high-speed system controller is coupled to the low-speed I/O controller (figure 4). As stated in the Office Action, Iachetta does not disclose that the high-speed arbiter is physically integrated into the system controller; therefore, Iachetta alone does not disclose that the high-speed arbiter coupled to the low-speed I/O controller. Kelly's bridge has an integrated arbiter (figure 3, structure 102) to arbitrate bus access. Kelly teaches one to integrate the arbiter into the bridge to arbitrate bus access according to the priority. Hence, the

combination of the prior arts does disclose that the high-speed arbiter coupled to the I/O controller.

7. In response to Applicant's argument that the claims do not claim a high-speed system controller or a low-speed I/O controller (Remark, page 5, 1st paragraph, lines 9-10): The claimed limitations of the claim 18 explicitly recite a system controller having a high-speed bus arbiter and an I/O controller having a low-speed bus arbiter; thus, the claims do claim a high-speed system controller and a low-speed I/O controller.

8. In response to Applicant's argument that if one were to combine the teaching of Kelly with Iachetta, as best understood, the result would simply be a single host bridge with switching logic as taught by Kelly with no need for the claimed I/O controller (Remark, page 5, last paragraph): Kelly's bridge has an integrated arbiter (figure 3, structure 102) to arbitrate bus access. Kelly teaches one to integrate the arbiter into the bridge to arbitrate the bus according to the priority. Kelly's teaching on the component integration does not teach away from Iachetta. The practice of the component integration will not defeat any of Iachetta's functions since each arbiter remains arbitrating the bus assess requests to its associated bus. Although Kelly discloses an embodiment without explicitly including separate system controller, the related part of the Rejections above only applies Kelly's teaching on the integration of an arbiter and a bridge, not the management of the separate bus speeds with one single bridge. Regarding the claim 24, the claim 24 recites an I/O controller connecting to both a high-speed peripheral bus and low-speed peripheral bus, which is a single bridge connecting to different buses with different speeds as taught by Kelly.

Conclusion

7. The prior art made of recorded previously and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,175,889 to Olarig: Olarig discloses that a CD ROM is a known storage device attached to an I/O controller.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
November 14, 2005

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/14/05